ELECTRONICS

M.Sc. Physics

PRACTICAL -II

FIRST YEAR, SEMESTER-II, PAPER-VI

LESSON WRITER
Prof. Sandhya Cole
Department of Physics,
Acharya Nagarjuna University,

EDITOR
Prof. Ch. Linga Raju
Department of Physics,
Acharya Nagarjuna University

ACADEMIC ADVISOR
Prof. R.V.S.S.N. Ravi Kumar
Department of Physics,
Acharya Nagarjuna University,

DIRECTOR, I/c.
Prof. V. Venkateswarlu
M.A., M.P.S., M.S.W., M.Phil., Ph.D.
CENTRE FOR DISTANCE EDUCATION
ACHARYA NAGARJUNA UNIVERSITY
NAGARJUNA NAGAR 522 510
Ph: 0863-2346222, 2346208
0863- 2346259 (Study Material)
Website www.anucde.info
E-mail: anucdedirector@gmail.com

M.Sc. Physics: Electronics Practical

First Edition : 2025

No. of Copies :

Published by:

Prof. V. VENKATESWARLU
Director, I/c
Centre for Distance Education,
Acharya Nagarjuna University

Printed at:

FOREWORD

Since its establishment in 1976, Acharya Nagarjuna University has been forging ahead in the path of progress and dynamism, offering a variety of courses and research contributions. I am extremely happy that by gaining 'A+' grade from the NAAC in the year 2024, Acharya Nagarjuna University is offering educational opportunities at the UG, PG levels apart from research degrees to students from over 221 affiliated colleges spread over the two districts of Guntur and Prakasam.

The University has also started the Centre for Distance Education in 2003-04 with the aim of taking higher education to the door step of all the sectors of the society. The centre will be a great help to those who cannot join in colleges, those who cannot afford the exorbitant fees as regular students, and even to housewives desirous of pursuing higher studies. Acharya Nagarjuna University has started offering B.Sc., B.A., B.B.A., and B.Com courses at the Degree level and M.A., M.Com., M.Sc., M.B.A., and L.L.M., courses at the PG level from the academic year 2003-2004 onwards.

To facilitate easier understanding by students studying through the distance mode, these self-instruction materials have been prepared by eminent and experienced teachers. The lessons have been drafted with great care and expertise in the stipulated time by these teachers. Constructive ideas and scholarly suggestions are welcome from students and teachers involved respectively. Such ideas will be incorporated for the greater efficacy of this distance mode of education. For clarification of doubts and feedback, weekly classes and contact classes will be arranged at the UG and PG levels respectively.

It is my aim that students getting higher education through the Centre for Distance Education should improve their qualification, have better employment opportunities and in turn be part of country's progress. It is my fond desire that in the years to come, the Centre for Distance Education will go from strength to strength in the form of new courses and by catering to larger number of people. My congratulations to all the Directors, Academic Coordinators, Editors and Lesson-writers of the Centre who have helped in these endeavors.

Prof. K. Gangadhara Rao
M.Tech., Ph.D.,
Vice-Chancellor I/c
Acharya Nagarjuna University.

M. Sc Physics
Semester-II, Paper-VI
PRACTICAL-II,
206PH24-ELECTRONICS

1. Inverting, Non inverting Summing Amplifier
2. Regulated DC Power Supply
3. Verification of truth tables of Logic gates
4. Combination of logic circuit by using universal NAND gate
5. First Order Active Filter
6. MOSFET
7. FET

CONTENTS

Experiment No. 1

INVERTING, NONINVERTING and SUMMING AMPLIFIER

AIM :- To study the working of op-Amp as Inverting, Non-inverting and Summing amplifiers.

APPARATUS: -

S.NO.	NAME OF THE ITEM	RANGE	QUANTITY
1.	DC Regulated Power Supply	±12V	1
2.	Digital multi meter	-	1
3	breadboard	-	1
4.	Op-Amp	IC-741	1
5.	Resistances	10 kΩ	3
		1 kΩ, 2.2 kΩ	
		3.3 kΩ,4.7 kΩ	1

Details of 741 OP AMP:

IC 741 is available in two packages. The pin configuration of 741 op-amp in dual in line package (DIP) is given below. It is the most commonly and widely used general-purpose op-amp. It has an integrated 30pF MOS capacitor. It has high input impedance (> 1M Ω), low output impedance (750 Ω) and large voltage gain (200,000).

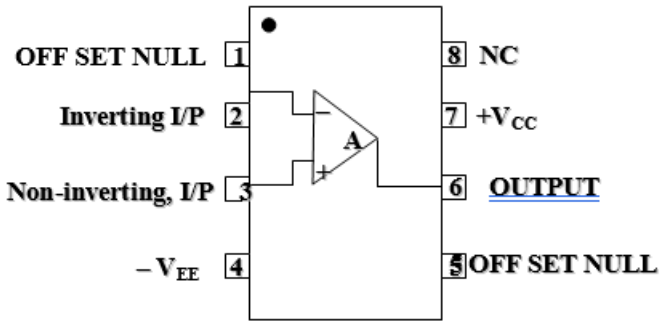


Fig 1.1: Pin configuration of μA-741 op-amp.

A dot on the top left corner is used to identify pin number 1. It needs a ±12V DC dual power supply. It is basically a high gain differential amplifier with two inputs.

Operational Amplifier:

An operational amplifier is a direct-coupled high gain amplifier usually consists of one or more differential amplifiers and usually followed by a level translator and an output stage. The output stage is generally a push pull or push pull complementary symmetry pair. An operational amplifier is available as a single integrated circuit package. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration. Thus, the name operational amplifier stems from its original use for doing these mathematical operations and so is abbreviated to op-amp. With the addition of suitable external feedback component, the modern-day operational amplifier can be used for a variety of applications. Such as AC and DC signal amplification, active filters, oscillators, comparators, regulators and others.

Schematic symbol:

The most widely used symbol for a circuit with two inputs and one out put is shown in fig (1. 2)

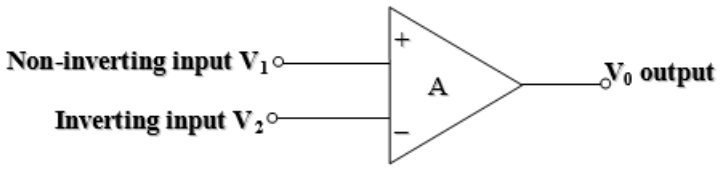


Fig. 1.2: Schematic symbol of op-amp.

In fig (1.2)

v_1 = voltage at the non-inverting input (volts)

v_2 = voltage at the inverting input (volts)

v_o = output voltage (voltage)

All these are measured w.r.t. ground

A = large signal voltage gain that is specified on the data sheets for an op-amp

power supply and other pin connections are not usually shown in circuits. Since the input differential amplifier stage of the op-amp is designed to be operated in the differential mode, the differential inputs are designated by the (+) and (-) notations, the (+) input is used for non-inverting input. An ac signal (or dc voltage) applied to this input produces an in-phase (or same polarity) signal at the output. On the other hand the (-) input is the inverting input because an ac signal (or dc voltage) applied to this input produces an 180 out of phase (or opposite polarity) signal at the output

Ideal op-amp:

An ideal op-amp exhibits the following electrical characteristics.

(1) Infinite voltage gain A_V.

(2) Infinite input resistance R_i, so that, almost any signal source can drive it and there is no loading of the preceding stage.
(3) Zero output resistance R_o, so that, output can drive an infinite number of other devices
(4) Zero output voltage when the input voltage is zero.
(5) Infinite bandwidth, so that, any frequency signal from 0 to $\propto$ Hz can be amplified with out attenuation.
(6) Infinite common mode rejection ratio so that output common mode noise voltage is zero.
(7) Infinite slew rate so that voltage changes occur simultaneously with input voltage changes.

There are practical operational amplifier circuits that can be designed to achieve many ideal characteristics by using a negative feedback arrangement. In particular, the input resistance, output resistance, and bandwidth can be made close to their ideal values through this method. Since the open-loop gain of an op-amp is extremely high, only very small signals (of the order of microvolts or less) and of very low frequency can be amplified accurately without distortion. However, signals of such small magnitude are highly susceptible to noise.

In addition to being very large, the open-loop gain of an op-amp is not constant. The voltage gain varies with changes in temperature, power supply, and manufacturing processes. These variations in voltage gain are relatively large in open-loop operation, making the open-loop op-amp unsuitable for most linear applications. In linear applications, the output is proportional to the input and of the same type.

Furthermore, the bandwidth (the range of frequencies over which the gain remains constant) of most open-loop op-amps is extremely small—almost negligible. Therefore, open-loop op-amps are impractical for AC applications. For example, the open-loop bandwidth of the 741C op-amp is approximately 5 Hz. However, most AC applications require a bandwidth much greater than 5 Hz.

Because of the reasons stated above, the open-loop op-amp is generally not used in linear applications. Nevertheless, in certain applications the open-loop op-amp is deliberately used as a nonlinear device; that is, a square-wave output is obtained by intentionally applying a relatively large input signal. Open-loop op-amp configurations are most suitable for such applications.

The gain of an op-amp can be selected and controlled by introducing a modification in the basic circuit. This modification involves the use of feedback, in which a portion of the output signal is fed back to the input either directly or through another network. If the feedback

signal is of opposite polarity or is 180° out of phase with respect to the input signal, the feedback is called negative feedback.

An amplifier with negative feedback has a self-correcting ability to counteract changes in output voltage caused by variations in environmental conditions. Negative feedback is also known as degenerative feedback because its use reduces the output voltage amplitude and, consequently, the overall voltage gain.

The inverting amplifier with negative feed back:

In the inverting amplifier only one input is applied and that, to the inverting input terminal. The non-inverting input terminal is grounded. Since $v_1 = 0$ and $v_2 = v_{in}$.

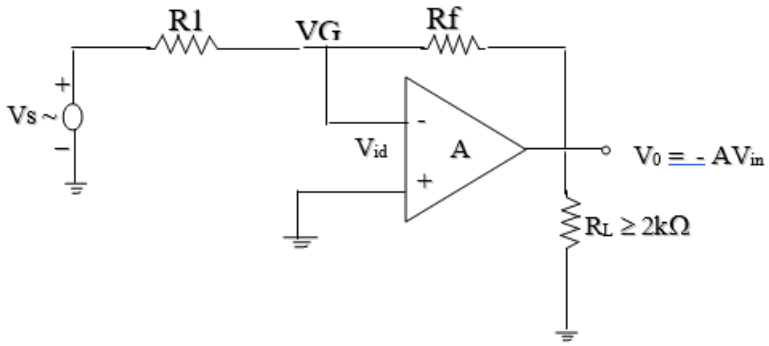


Fig 1.3: Inverting amplifier..

The negative sign indicates that the output voltage is out of phase with respect to input by 180^0 or is of opposite polarity. Thus in the inverting amplifier the input signal is amplified by gain A and is also inverted at the output.

Gain of inverting amplifier with feed back:

As the non inverting input of the amplifier is grounded and as no current passes through the input resistance (it is assumed to be infinite in ideal case). The inverting input terminal also must be at zero potential as there cannot be any voltage drop across R_i.The junction point of R_1 , R_f and inverting input is called virtual ground. Therefore

the input current $I_i = \frac{V_s}{R_1}$

flows through Rf resulting in a voltage drop = $R_f * I_i = -V_o$.

Therefore $V_o = R_f \times (-V_s / R_1) = -(R_f / R_1) \times v_s$

Voltage gain $Av = V_o/V_i = -(R_f / R_1)$

The expression for voltage gain doesn't contain any parameter pertaining to OP AMP. If $R_f = R_1$. The input and output signals have equal amplitude but differ in phase by 180º. It is called inverting unity gain amplifier. If the ratio R_f/R_1 is varied the output signal amplitude can be scaled up or down. In this application it is called scale changer. Because of virtual ground

mentioned above any signal connected to the inverting input through a resistance $R_x = R_1$ supplies current independent of other sources. The current flowing through R_f is algebraic sum of the currents entering in the node. As a result the output voltage can be considered as sum of input signal amplitudes. In this configuration such an amplifier is called summing amplifier. Any number of input signals can be connected like this and the output voltage of the summing amplifier is

$$v_o = -\frac{R_f}{R}(v_1 + v_2 + ..v_x + ..v_n)$$

The non-inverting amplifier:

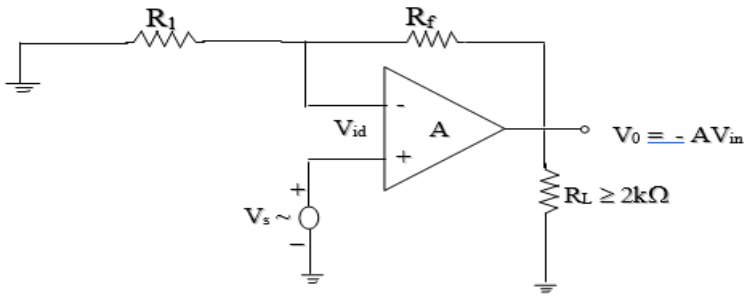


Fig 1.4: Non-Inverting amplifier.

Fig 1.4 shows the open loop configuration of non inverting amplifier. In this configuration the input is applied to the non inverting input terminal and the inverting input terminal is grounded.

In the circuit shown below $v_1=v_{in}$ and $v_2=0v$. Therefore, according to equation $v_0 = Av_{in}$. This means that the output voltage is A times larger than the input voltage and is in phase with input signal. The type of feedback involved is called voltage series feedback. The circuit 1.4 is redrawn to show feedback.

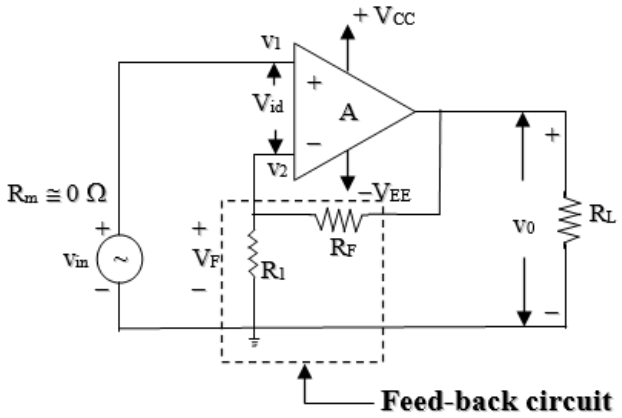


Fig 1.5: Voltage series feed back amplifier.

Expression for voltage gain:

As the input resistance of the amplifier is infinite, the inverting terminal will be at same potential as that of the non-inverting input. The current flowing through the resistance R_f is $(v_o-v_1)/R_f$. It must be equal to v_1/R_1 in magnitude. Equating

$$\frac{v_1}{R_1} = -\frac{(v_1 - v_o)}{R_f}$$

we can rewrite it as

$$v_1\left(\frac{1}{R_f} + \frac{1}{R_1}\right) = \frac{v_o}{R_f}$$

The voltage gain

$$A_v = \frac{v_o}{v_s} = 1 + \frac{R_f}{R_1}$$

In this configuration output signal will be in phase with input..For $R_1=R_f$ the gain is 2.

PROCEDURE:-

INVERTING AMPLIFIER:-

1. Select R_f and R_1 depending on the gain required. Connections are made as per the circuit diagram. Use low wattage resistors preferably one eighth watt so that resistance leads smoothly fit into the breadboard. When high wattage resistors are used in a circuit do not use them in bread board. Use separate group board for them.

2. Fix the IC741 on breadboard such that pins insert in the holes without bending. Enough care must be taken while inserting and removing ICs from bread boards and sockets. Better use IC inserters and Plucker's for this.

3. Use minimum length of wire to make connections. The gauge of the wire is selected such that it goes into the whole smoothly. Bent wires should not be inserted. Use a wire cutter cum sleeve remover to ut bent ends and to remove plastic sleeve. Use various colours of wires so that the connections can be identified easily. Use common ground. If several ground points are used ensure that they are all common by checking resistance between those points.

4. Use fixed voltage DC power supply preferably SMPs. The +12 V DC line is given to pin No. 7. –12V DC is given to pin No. 5. Fix the For inverting amplifier vary the input

voltage from 1 to 6 v in steps of 1v and measure the output voltage as a function of the input voltage ..Compare the experimental gain with the total gain of $-R_F/R_1$

S.No.	R_1	Output Voltage		Gain	
		Practical	Theoretical	Practical	Theoretical

SUMMING AMPLIFIER:-

1. Apply $V_1$and varyV_2 from .5 to 2.5v in steps of .5measure the output voltage with the help

S.No	Input voltage		Output voltage	
	V_1	V_2	Theoretical	Practical

of multimeter.

2. Compare the experimental values with the theoretical values.

NON-INVERTING AMPLIFIER: -

1.Apply the input voltage to the non-inverting terminal from 0.5 to 2.5 in steps of 0.5V measure the output voltages.

2. Compare the practical and theoretical values.

S.No.	R_1	Output Voltage		Gain	
		Practical	Theoretical	Practical	Theoretical

PRECAUTIONS:

1) Check the IC for corking by using it in inverting amplifier.

2) Ensure common ground for all ground connections.

3) Some function generators may have offset null facility. Use it if no output signal is observed even after circuit is assembled properly.

RESULT: -

We observed that the OP-AMP is used as an inverting, non-inverting and summing amplifiers.

Experiment No. 2

DC REGULATED POWER SUPPLY

Aim: To construct a regulated power supply using a transistor and study its performance.

Apparatus: Transistor BC107, ECN 055 power transistor, resistance box, 0-500 milliammeter, Dimmerstat

Theory:

A DC power supply, constructed using a full wave rectifier with filter circuit still suffers with some disadvantages like

1. Poor regulation: If the DC output voltage varies with load current it is said to have poor regulation.
2. The DC output voltage varies with AC line voltage.
3. The DC output varies with temperature.
4. The ripple voltage, though reduced by filter, the dc voltage is not completely free from it.

To overcome these difficulties a regulator is introduced between the unregulated supply and the load. The following are some of the types of regulators

1. Shunt regulators
2. Series regulators
3. Switching regulators.

Here we discuss the construction of a regulated power supply using series regulator. The series transistor T_1 (called pass transistor) is operated as an emitter follower and appears in series with the load resistance. Hence this regulator is called series regulator. In series regulator the regulation is achieved by comparing a sample of output voltages with a reference voltage. The reference voltage is taken across a zenor diode (V_z). The comparison is carried out by dc amplifier, which produces a signal proportional to the difference between sample voltage and Vz (zener voltage).

A part of the output voltage V_o is sampled by means of the potential divider R_1 and R_2 (see FIG 1). The voltage across R_2 $=\beta V_o$ where $\beta = (R_2/R_1 + R_2)$. This fraction of output is fed to the base of the transistor T_2. The emitter of T_2 is connected to the Zener diode and therefore is at a fixed voltage, V_z, which is the reference voltage.

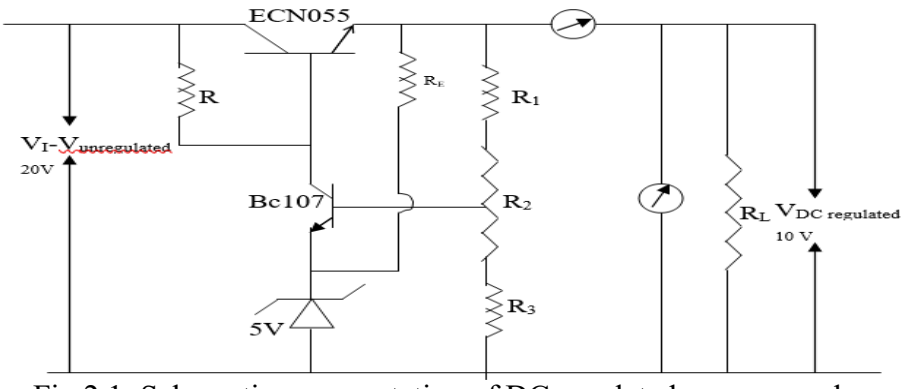


Fig.2.1: Schematic representation of DC regulated power supply.

Due to any reason let the output voltage V_0 go up. Then βV_0 also goes up. Thus the base- emitter voltage of T_2 goes up. This will increase the base current of T_2 and consequently collector current of T_2 also increases. This increases the voltage drop across the collector resistance R of T_2 due to its increased collector current. This decreases the bias voltage of T_1. Due to emitter follower function the emitter voltage of T_1 decreases. Thus, this is a change in opposite to the original change of V_D. Thus, the output voltage remains constant.

Regulation with load:
Procedure:

1. Connect the circuit as shown in the figure.
2. Before making connections, we have to identify the collector and emitter and base of the power transistor ECNO55.
3. Connect an unregulated power supply of 20 V DC (see Fig 2) to the regulator section. Keep the ac input to the unregulated supply at 220V AC Adjust the output voltage to 10V DC by varying the potentiometer.
4. By varying R_L measure the output voltage as a function of load current. Change the load resistance such that the load current changes in steps of 10mA.
5. The input and output voltages are measured by using digital multimeter

Regulation with line voltage:

1. Fix the load current at an optimum value say 50mA.
2. By using a Variac (Dimmerstat) change the AC input of unregulated supply in steps of 10V from 210 – 260 V. In each case measure the input and output voltages.
3. A graph is drawn by taking line voltage along X-axis and unregulated input and regulated output voltages along Y-axis.

% of regulation is defined as the percentage change in output voltage when load is removed

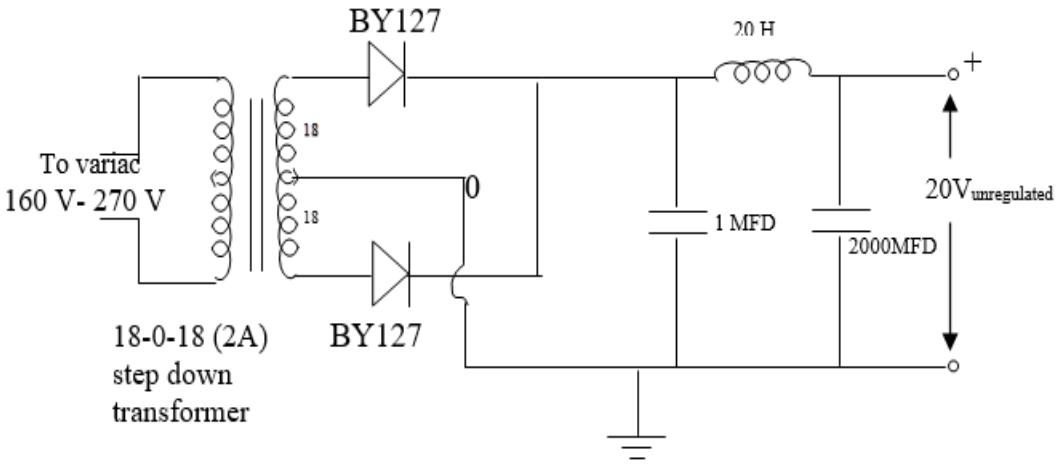


Fig. 2.2: unregulated dc supply.

Observations:
Regulation with load current:
% of regulation= $(E_{0\ noload}-E_{\ 0\ full\ load})/E_{0\ full\ load}$

Unregulated input voltage without load = Volts

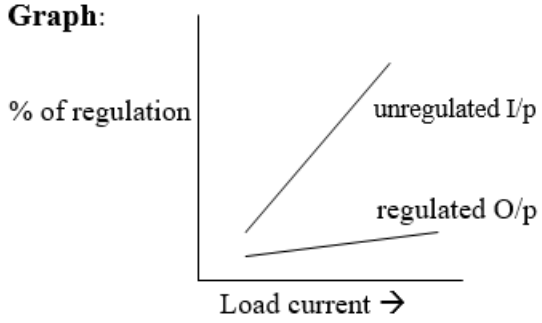
Regulation with line voltage at load current 300 mA

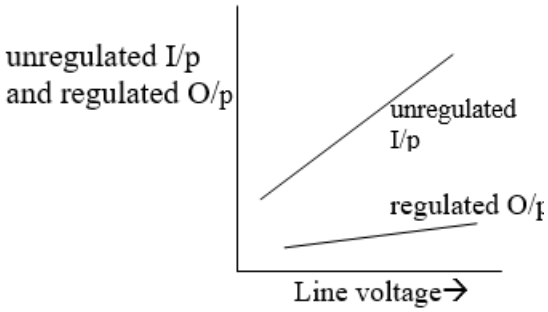
Sl.no.	Line voltage (V)	Unregulated input voltage (V)	Regulated output voltage(V)

The unregulated output voltage without load = Volts

For the ECN055 body of the transistor acts as collector. When fixed to metal chassis its body must be isolated from ground through graphite spacer. A heat sink will enable to draw large current (500mA).

Graph:





Precautions:

1. Measure the voltages with the same meter and in the same setting.
2. Do not use a decade resistance box as load box as the resistances are not meant for high current use. The resistance may be burned and thereby will spoil the box.
3. Connect the unregulated power supply which has the required current delivering capacity to the regulated supply section.

Result:

A transistorized version of dc power supply voltage 10 V is constructed and its regulation with load current up to 450 mA line voltage is studied.

Note: Students may be asked to study regulation at different output voltages.

Students may be asked to study the variation of output voltage with change in reference voltage(by changing Zener diode.).

Students may be asked to study the performance of the circuit with and without heat sink to series pass transistor.

Experiment No. 3

VERIFICATION OF TRUTH TABLES OF LOGIC GATES

Aim: To study the function of various logic gates by verifying their truth tables.

Apparatus: IC`s with numbers 7432,7400,7402,7404,7408,7486. Bread board, 5V DC power supply, LEDs.

Theory:

Existence of positive voltage at a point may be taken as logic 1. Zero voltage can be represented as logic 0. A glowing bulb, a current flow, a happening of an incident can be represented by logic 1 or TRUE state. The complementary actions can be represented by a 0 or FALSE state. In fact actions that were represented by 1 may also be represented by 0. It all depends on one's choice. The electronic circuits used to perform Boolean operations are called gates. The gate is a circuit with one or more input signals but only one output signal. These gates are constructed by using diodes and transistors (known as DTL logic) or using transistors only (known as TTL). Technical standards were evolved in electronics depending on the implementation of integrated circuits using various semiconductor technologies viz DTL,TTL,ECL etc. The most important and popular semiconductor logic is Transistor-Transistor Logic (TTL), in which a +5V DC is taken as logic 1 and zero volts is taken as logic 0. We learn the fundamentals of Boolean operations, corresponding logic circuits and gates and integrated circuits related to these circuits.

1. Boolean Algebra :

The fundamental operations in Boolean algebra are OR, AND and NOT, with symbols + (plus), **.** (dot) and bubble or bar over Boolean variable respectively.

In real life applications, one combines several logic gates and the combined effect determines a system behavior depending on the states of individual logic variables. This is usually expressed in terms of a truth table. In truth table, various inputs are listed and various combinations are worked out to determine the system behavior. As a simple example, see the OR gate truth table given in table(a). Here A and B are the input variables. These two variables can have 2^2=4 combinations of 1s and 0s. As per the Boolean equation y = A + B (A+B to be red as A or B), output is true for 3 input combinations and false for one combination.

The following are the laws of Boolean algebra and complicated laws can be proved using simple Boolean laws. These laws can be verified by writing truth tables for L.H.S and R.H.S expressions.

1. $A + 0 = A$
2. $A + 1 = 1$
3. $A + A = A$
4. $A + \overline{A} = 1$

} Laws of 'OR'

5. $A \cdot 0 = 0$
6. $A \cdot 1 = A$
7. $A \cdot A = A$
8. $A \cdot \overline{A} = 0$

} Laws of 'AND'

a. $\overline{0} = 1$

9. $\overline{1} = 0$
10. of $A = 0$ then $\overline{A} = 1$

} Laws of complementation (NOT Laws)

2. Basic logic gates:

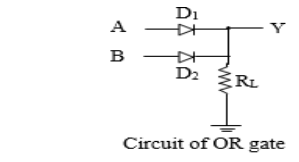
Basically, a logic gate is a circuit with one or more logic input signals (each input is either 0 or 1), but with only one output signal (logically related to inputs). Logic circuits are analyzed with the help of Boolean laws.
The basic logic gates are: OR, AND and NOT

OR Gate:

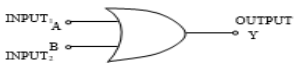
An OR gate has two or more input signals but only one output signal. If one or more input signals are high, the output signal is high.

Boolean expression for two input OR gate is $Y = A + B$ (read as Y equals A OR B).

The circuit to implement the OR function, logic symbol and its truth table (which depicts the output condition to given input is shown in fig (a).



Circuit of OR gate

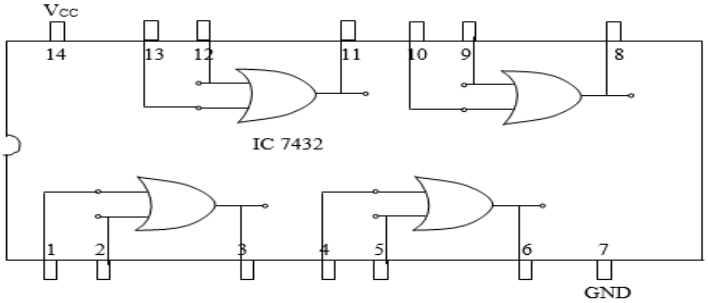


Logic Symbol of OR gate

Fig (a)

TURTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



Any one or both of the inputs A, B are high (+5V) makes the corresponding diode to forward bias and the current flows through load resistor R_L to have an output at Y.

An OR gate can have any number of inputs 1 to n. For example two input OR-gates can be used to form a 3 input OR gate as shown in fig (b)

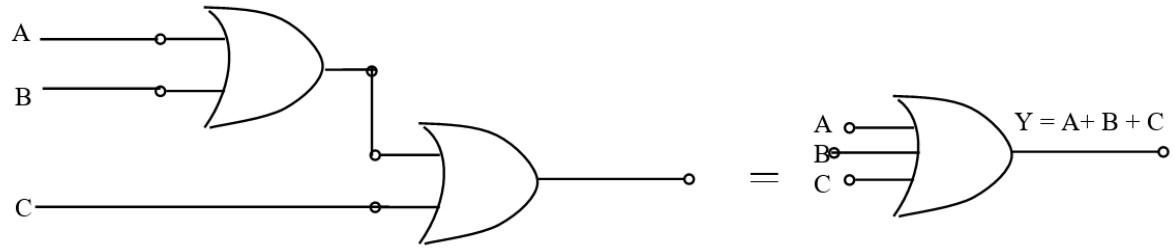
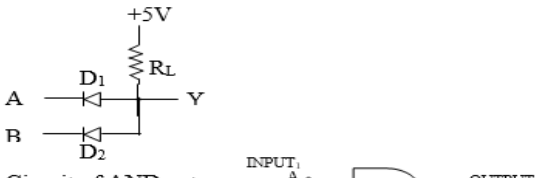


Fig b: Two input OR gates connected to form a 3-input OR gate.

The OR gate circuit of Fig (a) constructed by using diodes and resistors. But the same OR gate can also be constructed by using transistors only (TTL circuit). The logic gates are available in the form of integrated circuits (ICs) to offer advantages in terms of size, cost and power. The IC 7432 is a quad (four), two input OR gate using TTL logic and 74LS32 and 74HS32 are the low power and high speed versions of the same OR gate.

AND gate:

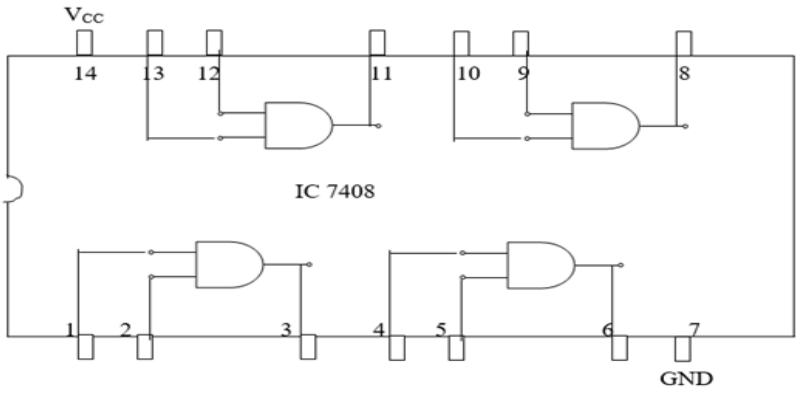
The AND gate has two or more inputs but has only one output. If all the inputs are simultaneously high, the output is high. Boolean expression for two input AND gate is $Y = A \cdot B$ (read as Y equals A AND B). The circuit to implement AND function, corresponding logic diagram and its truth table is shown in Fig (c)



TURTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Fig(c)



When any one or both of the inputs in above circuit are low, the diode of that input becomes forward biased, so the level of voltage at output point Y is at 0V i.e low state. On the other hand, if both A and B are high, both diodes are now reverse biased and having same voltages at both ends. So 5V appears at Y, i.e high state.

As in the case of OR gate, the two input AND gates can be used to construct three input or n-input AND gate. Construction of 3-input AND gate by using two 2-input AND gates is shown in Fig (d).

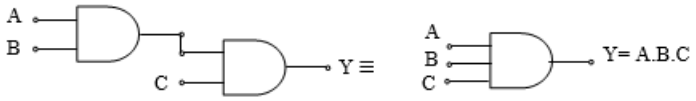


Fig (d)

NOT gate: (Inverter gate):

The inverter is a gate with only one input and one output. The output sate is always the opposite of the input state. It is also called as NOT gate. Boolean expression for this gate is $Y = \overline{A}$ (read as Y equals complement of A or Y equals NOT of A). The circuit, logic symbol and its truth table is shown in Fig (e).

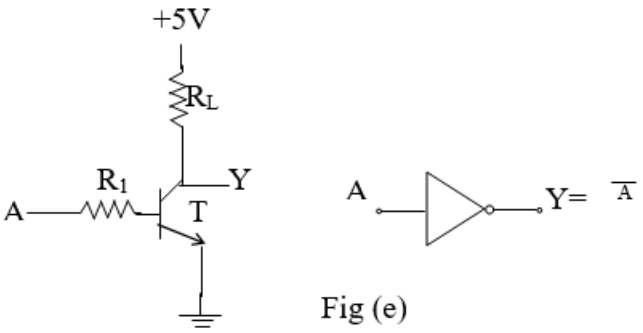
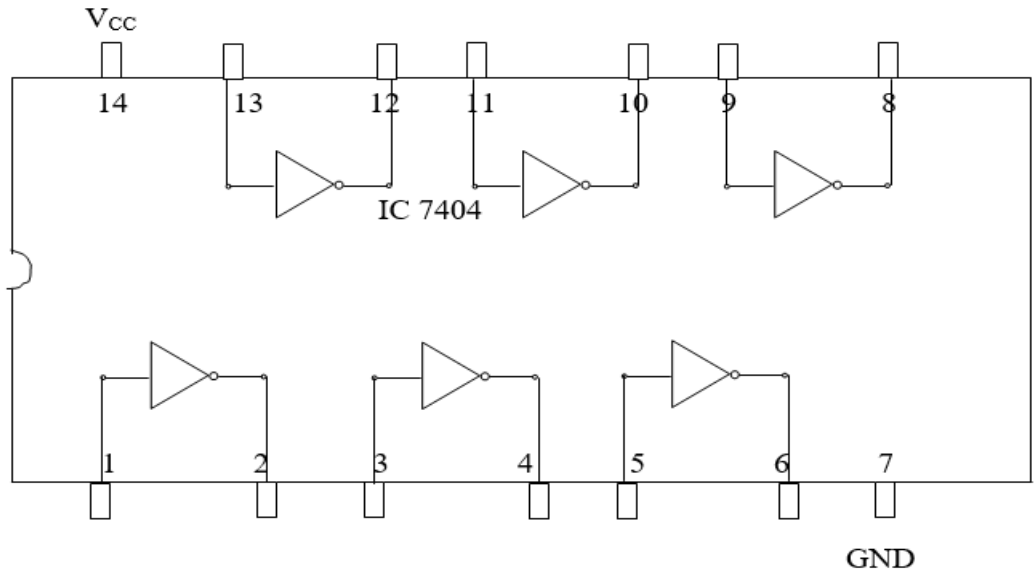


Fig (e)

TRUTH TABLE

Input A	Output Y
0	1
1	0



In the above circuit, the transistor is working either in the conduction or cut-off state. When a high state(+5V) is presented in the input, it makes the transistor to conduct and produce 0V or low state of output. On the other hand, a low state at A produces a high state at y by cut-off the transistor T.

Input given to Two NOT gates connected in cascade results in the original Boolean variable as shown in fig (f). This is called a buffer.

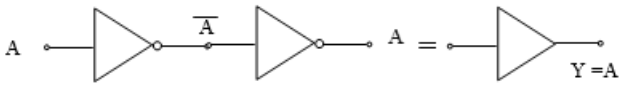


Fig (f) Two NOT gates connected to form a buffer, logic symbol of buffer and truth table

TRUTH TABLE

Input A	Output Y
0	0
1	1

Electronically buffers are very useful as they do not alter the nature of original signal but provides boosting of signal amplitude and power to standard levels. This prevents logic failure due to fall in signal strength. Tri-state buffers are also available whose output can be 0, or 1 or tri-state. In the tri-state condition the signal path is disconnected. These tri-state buffers are used in advanced logic circuits like Microprocessors and memories.

NOR gate:

The basic logic circuits are used to construct some more gates to perform more Boolean functions. For example, consider the NOR gate which has two or more inputs but only one output. All the inputs must be low to get a high output. Boolean expression for two input NOR gate is $Y = \overline{A + B}$.(read as Y equals not of A OR B).

The NOR gate can be constructed by connecting an OR gate with NOT gate as shown in Fig (g)

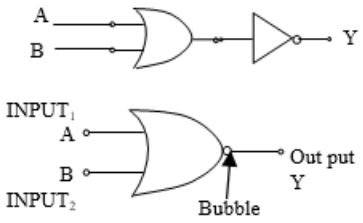
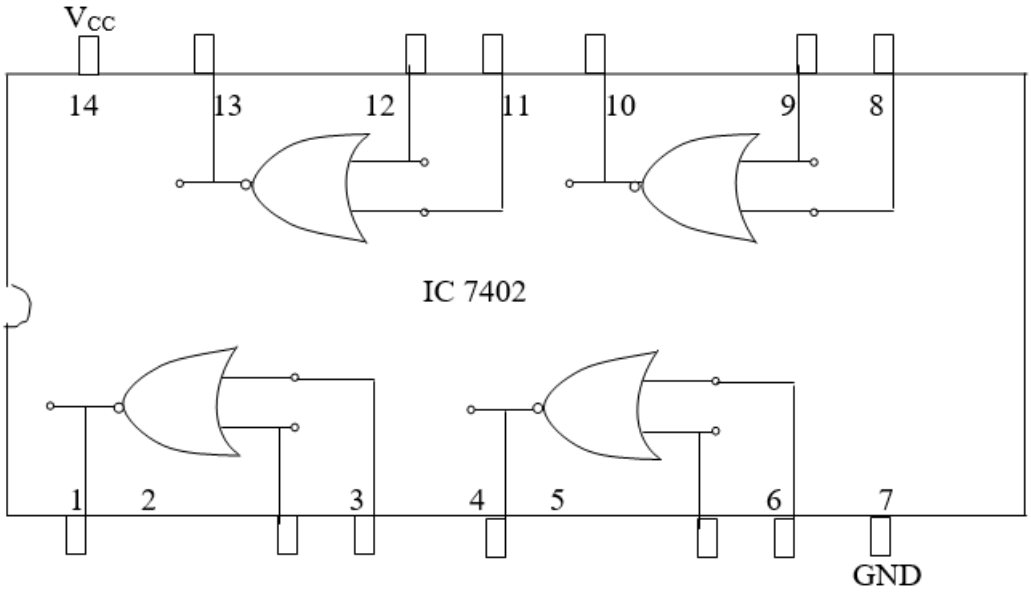


Fig (g)

TRUTH TABLE

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

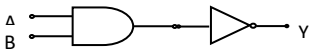
The



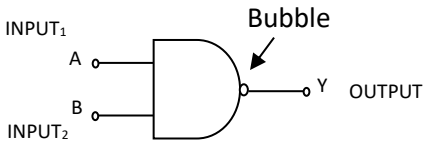
NOR gate may have more than two inputs. Regardless of how many inputs a NOR gate is still logically equivalent to one OR gate followed by an inverter. For instance, the equation for 3-input NOR gate is $Y= \overline{A+B+C}$. The 7402 is a quad 2-input NOR gate where as 7427 is a triple 3-input NOR gate.

NAND gate:

A NAND gate has two or more inputs but only one output. All the input are the simultaneously high to get a low output. Boolean expression for two – input NAND gate is $Y = \overline{A.B}$ (read as Y equals Not of A AND B).



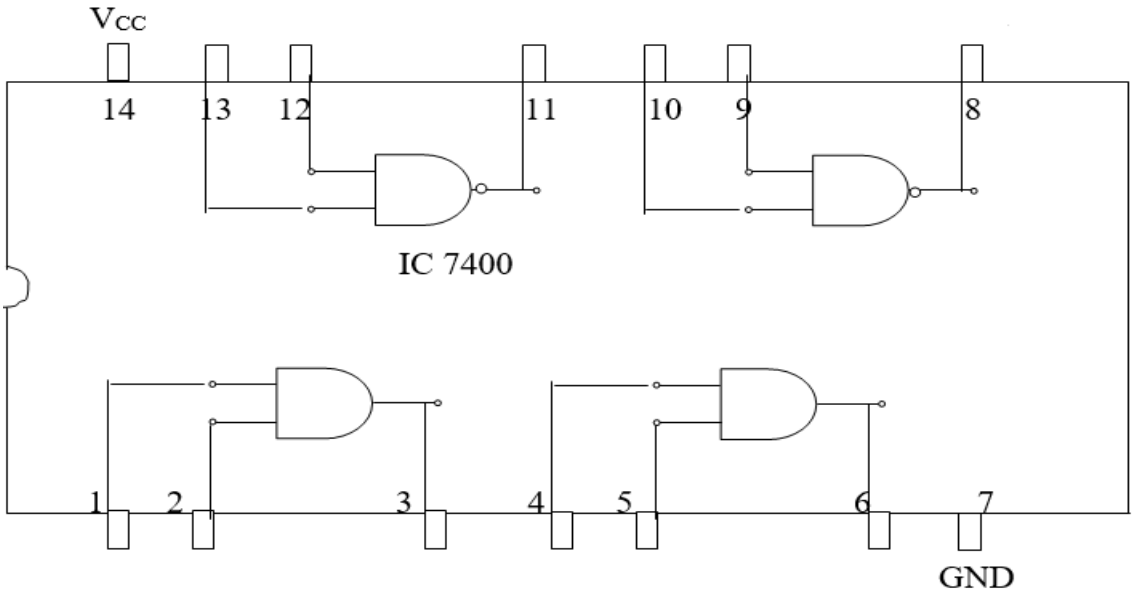
The Boolean equations for 3-input and 4-input NAND gates are $Y = \overline{ABC}$ and $Y = \overline{ABCD}$ respectively.



Logic Symbol of NAND gate

Fig (h)

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1



The IC 7400 have four 2-input NAND gates, whereas 7410 have three numbers of 3-input NAND gates.

EX – OR gate:

An OR gate recognizes words with one or more 1s, whereas the exclusive – OR gate recognizes only words that have an odd number of 1s. Boolean expression for two – input

EX-OR gate is $Y = A\overline{B} + \overline{A}B = A \oplus B$ (read as Y equals A EX-OR B). The logic diagram, symbol and its truth table is shown in Fig (i).

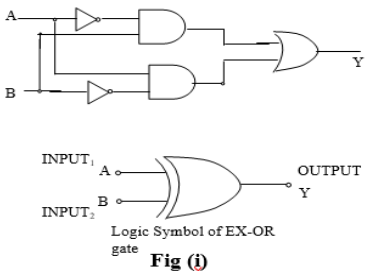
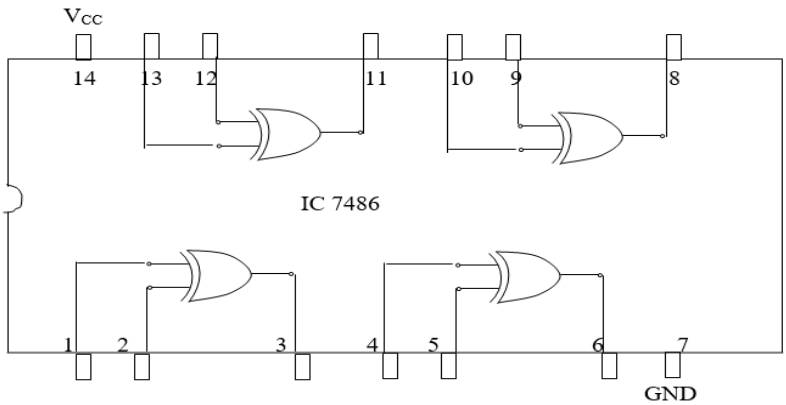


Fig (i)

TRUTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



When both inputs A & B in the above circuit are high or low both AND gates have low outputs to have the final output zero. But when any one of the input(A or B) is high, the corresponding AND gate output is high. So the final output is one as shown in truth table. IC 7486 is the IC version of EX – OR gate.

Precautions:

1 Use only small length single strand wires of size that fit into the holes of bread board.
2 Don't use thick wires
3 Do not bend the wire ends while inserting in bread board.
4 As there is a possibility of 5V and 0V carrying wires very nearby don't use high current power supplies as the short circuit may damage the bread board.
5 If you want to connect an LED to the output, use always a 1K resistance in series with the diode.
6 Use only exact +5V DC supply while using digital ICs. Don't connect variable voltage supplies to ICs.

Result: The truth tables are verified for the following logic gates and they are observed to be as expected for these gates

Experiment No. 4

COMBINATION OF LOGIC CIRCUITS WITH NAND GATE

Aim: To construct various logic gates using universal building block NAND gate.
Apparatus: SN 7400 ICs, Bread board, 5VDC fixed power supply, LEDs., 1/8W resistors

Theory:

1 **Forming other logic gates using only NAND gates:**

(i) NOT gate: From the truth table of the NAND gate given in Fig 1,

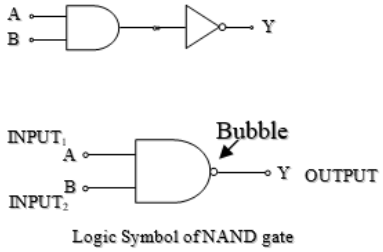


Fig 1

TRUTH TABLE

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

If all the inputs are connected to the same logic NAND gives its complement as output viz if A= B= 0 we have an output of 1 and if A= B= 1, the output is 0. Hence the circuit of Fig (a) acts as NOT gate.

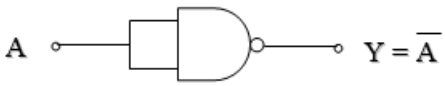


Fig (a)

$$y=\overline{A.A}=\overline{A}$$

ii) AND gate: The Boolean expression for NAND is Y= $\overline{A.B}$. Complimenting the output of NAND gate results in A.B the logical AND operation. So, in Fig b the first NAND gate output is $\overline{A.B}$ and second NAND gate simply connected as a NOT gate resulting in an AND gate circuit.

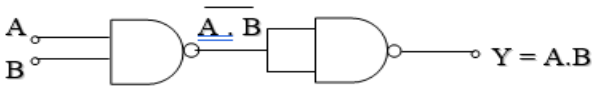


Fig (b)

$$y=\overline{\overline{A.B}}=A.B$$

iii) OR gate: The Boolean expression for logical OR operation is A+B. It can be written as $\overline{\overline{A}} + \overline{\overline{B}}$ Using De Morgan theorems it can be written as compliment of ($\overline{A}$. $\overline{B}$). Basically, it is an AND gate but the inputs are $\overline{A}$ and $\overline{B}$ instead of A and B. So two not gates to invert inputs and one NAND gate will generate OR operation as shown in fig c.

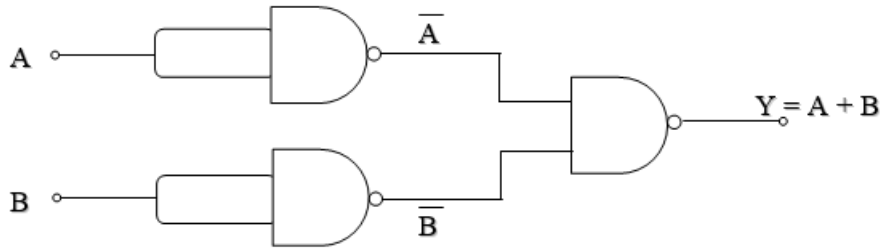


Fig (c)

(iv) NOR gate:

$$Y=\overline{\overline{A}.\overline{B}} = \overline{A} + \overline{B}=A+B$$

Addition of another NOT gate to the circuit for OR gate of Fig (c) as shown in Fig (d) gives the operation of a NOR gate.

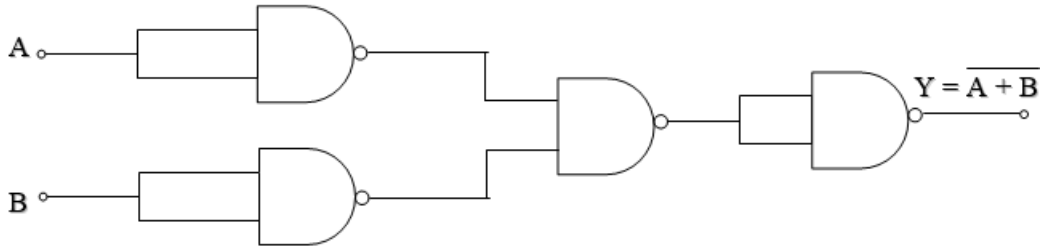


Fig (d)

$$Y= \overline{(A+B).(A+B)} =\overline{A+B}$$

(v) EX – OR gate: The Boolean expression is

$$Y = A\overline{B} + \overline{A}B$$

This equation can be expressed in various forms using De Morgan's laws.

Ex: $\overline{A}B+A\overline{B}$ can be expressed in NAND-NAND form as $\overline{\overline{A}.\overline{B}.\overline{B}.\overline{A}}$. this can be shown using only 4 NAND gates. The logic diagram is given in fig (e).

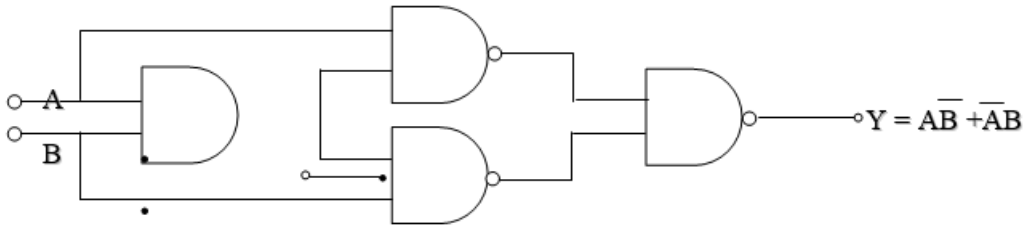


Fig (e)

$$\overline{A.\overline{AB}}=A.\overline{A}+\overline{B}=A\overline{B}$$

$$\overline{B.\overline{AB}}=B.\overline{A}+\overline{B}=B\overline{A}$$

$$Y=\overline{A.\overline{B}}.\overline{B.\overline{A}}=\overline{A.\overline{B}}+\overline{B.\overline{A}}=A\overline{B}+B\overline{A}$$

NOTE: the students may be asked to try other forms

2 Other Logic gates using only NOR gates:

(i) NOT gate: It is easy to verify from the truth table of NOR gate that when all the inputs of NOR are tied together it acts as an inverter.

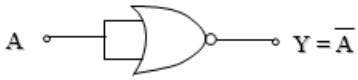


Fig (f)

$$Y=\overline{A+A}=\overline{A}$$

(ii) OR gate:

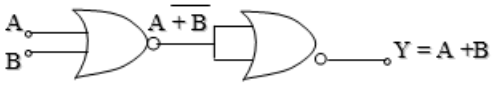


Fig (g)

$$Y=\overline{\overline{A+B}+\overline{A+B}}=\overline{\overline{A+B}}=A+B$$

(iii) AND gate:

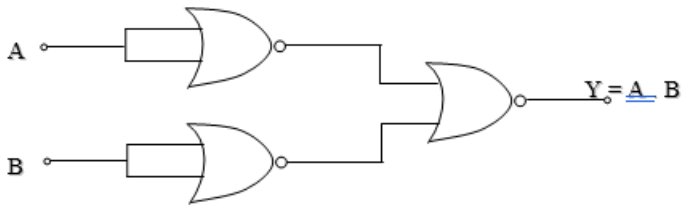


Fig (h)

$$Y=\overline{\overline{A+A}+\overline{B+B}}=\overline{\overline{A}+\overline{B}}=\overline{\overline{A}}.\overline{\overline{B}}=A.B$$

(iii) NAND gate:

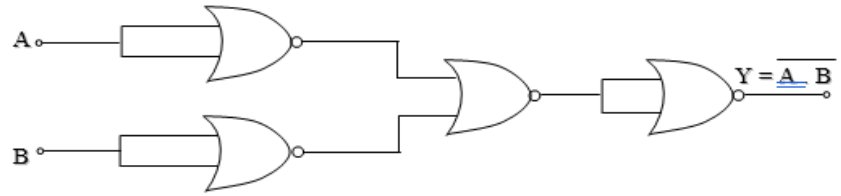


Fig (i)

$$Y'=\overline{\overline{A}+A+\overline{B}+B}=\overline{\overline{A}+\overline{B}}=\overline{\overline{A}}.\overline{\overline{B}}=A.B$$

$$Y=\overline{A.B+A.B}=\overline{A.B}$$

(v) EX - OR gate:

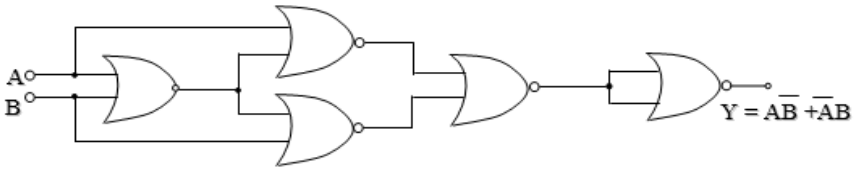


Fig (j)

$$Y'=\overline{\overline{A+\overline{A+\overline{B}}+B}+\overline{A+\overline{B}}}=\overline{\overline{A+\overline{A}.\overline{\overline{B}}+B}+\overline{A}.\overline{\overline{B}}}$$

$$=\overline{\overline{A}.(\overline{\overline{A}.\overline{\overline{B}}})+\overline{B}.(\overline{\overline{A}+\overline{\overline{B}}})}=\overline{A\overline{B}+B\overline{A}}$$

$$Y=\overline{Y'.Y'}=\overline{Y'}=A\overline{B}+B\overline{A}$$

Of the several technologies available Transistor–Transistor Logic is widely used where logic 1 is represented by +5V DC. And Logic zero by 0V DC. Circuits using other types of logic are provided with TTL logic compatibility to facilitate easy interfacing of logic circuits. When a logic gate is connected to another logic gate, depending on the logic status it is supposed to supply or take currents. Supplying current is called sourcing and taking the current is called sinking. Capability of a circuit depends on how much current a circuit can sink and source.

This is expressed in terms of how many logic gates can be connected to it (fan-in) and how many circuits can be driven by it (fan-out). For standard TTL fan – out is 10. Logic circuits are supposed to change their states from 0 to 1 or 1 to 0 instantaneously, but, electronic circuits have inherent delays and because of it, there will be some definite rise time, fall time and propagation delay as a signal passes from input to output. Further there will be signal attenuation and induction effects and noise, which affect signal amplitude. For a standard TTL circuit if a logic 1 signal amplitude falls below 2.4V DC it cannot be recognized as Logic1. Like wise, if logic 0 signal amplitude is greater than 0.4V DC it cannot be identified as logic 0. This results in failure of logic circuits. Crossing the fan-in and fan-out limits also changes logic voltages. So logic circuits are to be buffered to bring back, the signal levels to TTL levels before they are deteriorated. A signal in its transmission path may develop glitches, slopes and other types of distortion. Schmitt trigger circuit is used to produce rectangular wave shape regardless of the input waveform.

In many circuits the compliment of AND gate output is needed (0 is compliment of 1 and 1 is compliment of 0). It can be obtained by connecting NOT gate at the output of AND gate. The NAND gate diagram is as follows. This gate will give the inverted output or complement output of AND gate.

Precautions:

1. Verify the truth table of individual NAND elements in each IC before using them in the circuit.
2. The connections should be short and correct. Use different colored wires Ex Red for +5v, black for GND, Green for A, Blue for B input, Yellow for output. Select other colors as per your choice and availability.

Result: Truth tables of the constructed logic gates using NAND gate is verified along with ICs. The agreement is good.

Note:

1. Avoid any one of the connections
2. The truth tables should be verified for all the input combinations.

EXPERIMENT NO. 5

FIRST ORDER ACTIVE FILTERS

AIM:

To verify the various active filter circuits low pass filter, high pass filter, band pass filter and band reject filter.

APPARATUS:

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1	SIGNAL GENERATOR	(0-10)mHz	1
2	Op amp	IC741	3
3	Resistors	1kΩ,1.5kΩ, 5kΩ,10kΩ	2,1,2,4
4	Capacitor	0.1μf	4
5	linear power supply	±15V	1
6	DSO	-	-

THEORY:

Electronic filters are circuits which perform signal processing functions, specifically to remove unwanted frequency components from the signal, to enhance wanted ones, or both. Electronic filter high-pass, low-pass, band-pass, band-stop (band-rejection; notch), or all pass.

Active Low Pass Filter:

The most common and easily understood active filter is the Active Low Pass Filter. Its principle of operation and frequency response is exactly the same as those for the previously seen passive filter, the only difference this time is that it uses an op-amp for amplification and gain control. The simplest form of a low pass active filter is to connect an inverting or non-inverting amplifier.

High Pass Filter:

A first-order (single-pole) Active High Pass Filter as its name implies, attenuates low frequencies and passes high frequency signals. It consists simply of a passive filter section followed by a non-inverting operational amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier and for a non-inverting amplifier the value of the passband voltage gain is given as 1 + R2/R1, the same as for the low pass filter circuit.

Band Pass Filter:

The cut-off frequency or fc point in a simple RC passive filter can be accurately controlled using just a single resistor in series with a non-polarized capacitor, and depending upon which way around they are connected, we have seen that either a Low Pass or a High Pass filter is obtained. By connecting or “cascading” together a single Low Pass Filter circuit with a High Pass Filter circuit, we can produce another type of passive RC filter that passes a

selected range or "band" of frequencies that can be either narrow or wide while attenuating all those outside of this range. This new type of passive filter arrangement produces a frequency selective filter known commonly as a Band Pass Filter or BPF for short.

Unlike a low pass filter that only pass signals of a low frequency range or a high pass filter which pass signals of a higher frequency range, a Band Pass Filters passes signals within a certain "band" or "spread" of frequencies without distorting the input signal or introducing extra noise. This band of frequencies can be any width and is commonly known as the filters Bandwidth.

Band Reject Filter:

The Band Stop Filter, (BSF) is another type of frequency selective circuit that functions in exactly the opposite way to the Band Pass Filter we looked at before. The band stop filter, also known as a band reject filter, passes all frequencies with the exception of those within a specified stop band which are greatly attenuated.

If this stop band is very narrow and highly attenuated over a few hertz, then the band stop filter is more commonly referred to as a notch filter, as its frequency response shows that of a deep notch with high selectivity (a steep-side curve) rather than a flattened wider band.

The function of a band stop filter is too pass all those frequencies from zero (DC) up to its first (lower) cut-off frequency point fL, and pass all those frequencies above its second (upper) cut-off frequency fH, but block or reject all those frequencies in-between. Then the filters bandwidth, BW is defined as: (fH – fL).

Procedure:

1)Connect the circuit as shown in the diagram.

2)Connect the DSO to the probes and switch it on.

3)Check the graph for both positive and negative voltage and write down the output.

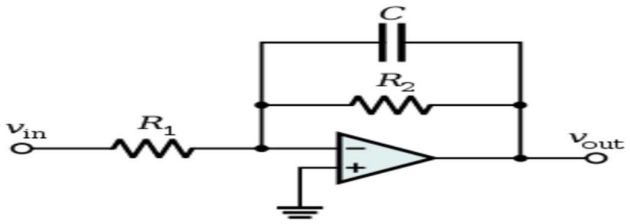
Design calculation:

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau}$$

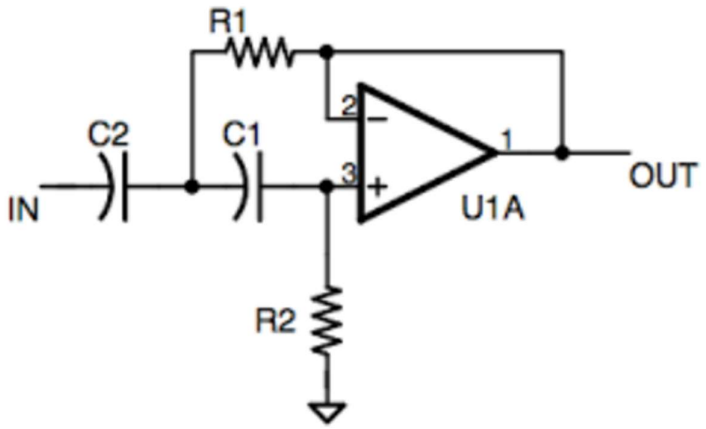
$$Gain = (+\frac{\boldsymbol{Rf}}{\boldsymbol{Ri}})$$

Circuit diagram:

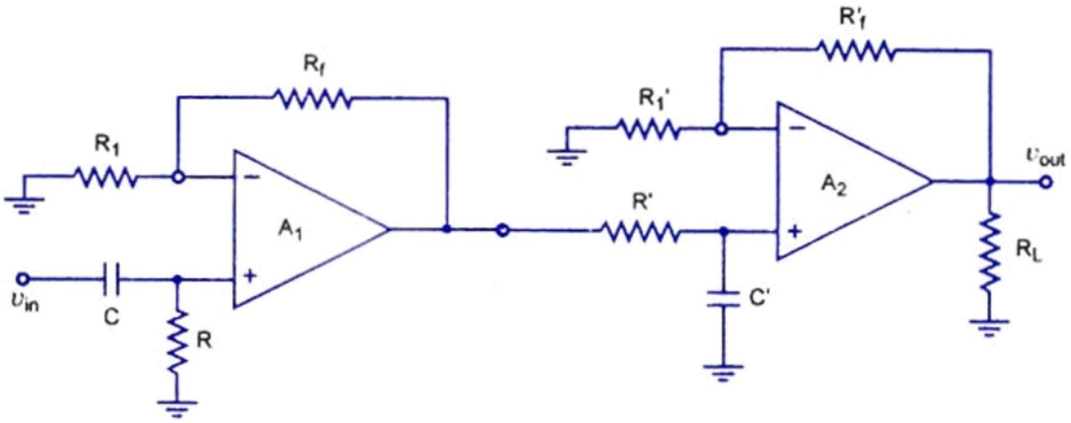
low pass filter:



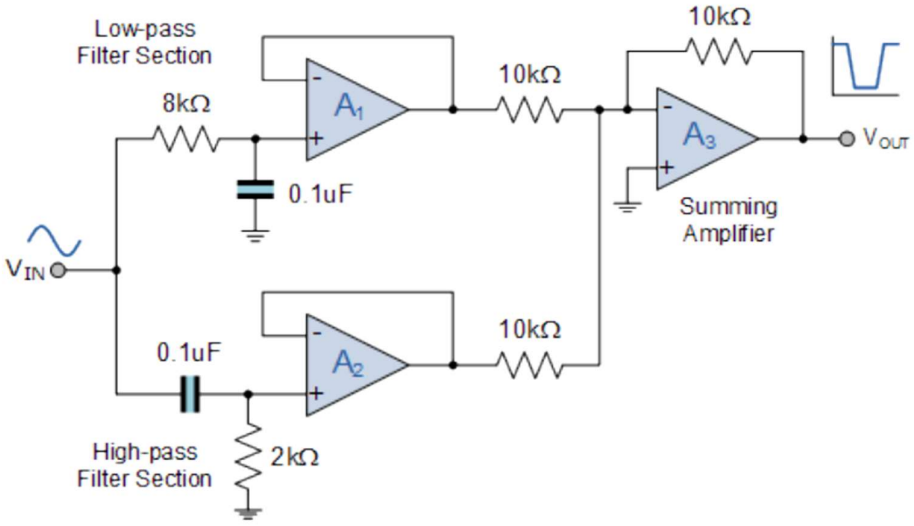
High pass filter:



Band pass filter:

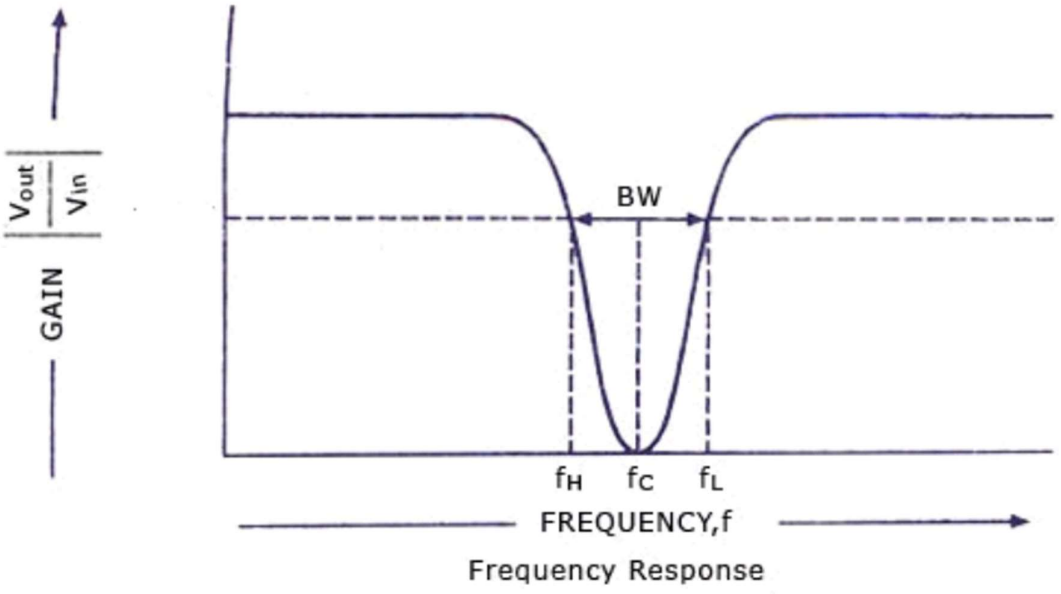


Band Reject filter:



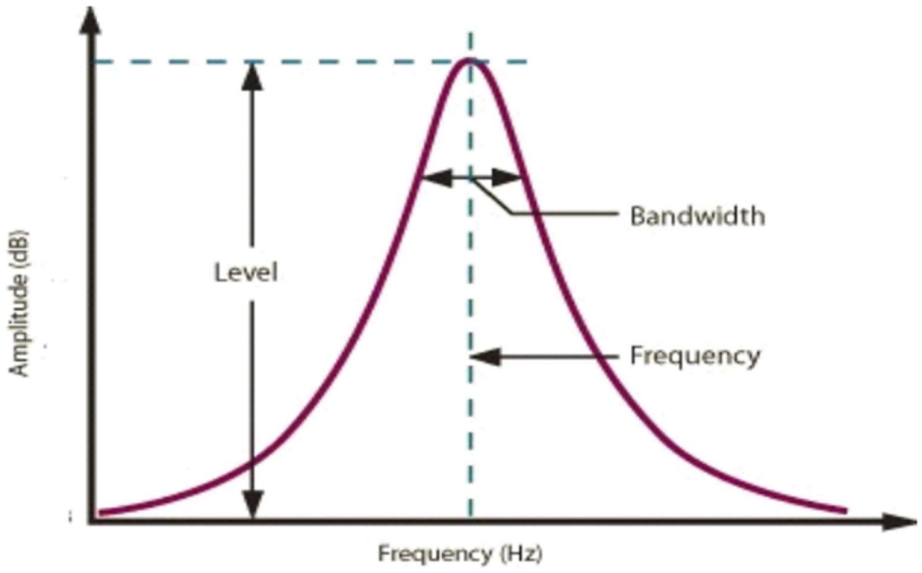
Model graph:

Band reject filter:

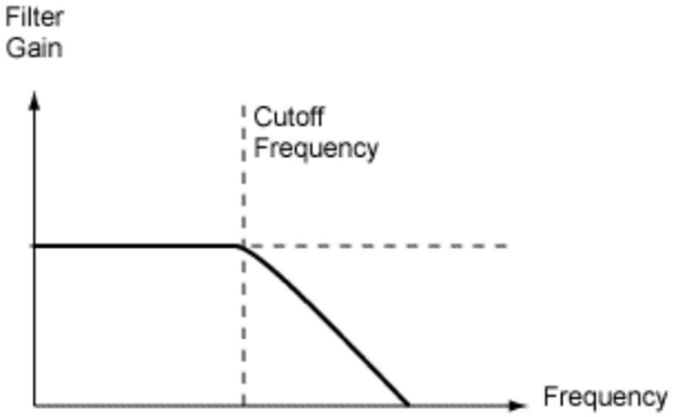


Frequency Response

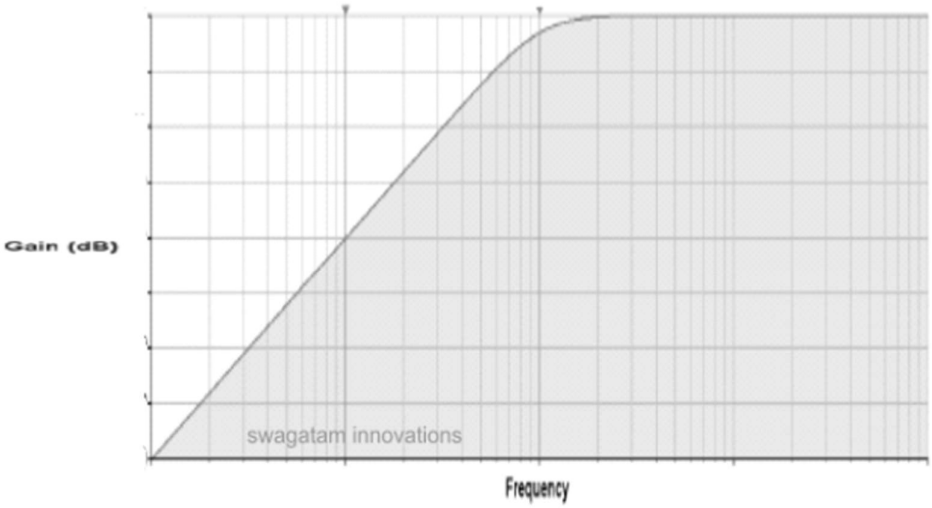
Band pass filter:



low pass filter:



High pass filter:



TABULATION:

LPF:

INPUT FREQUENCY(HZ)	OUTPUT VOLTAGE(V)	GAIN	GAIN IN dB

HPF:

INPUT FREQUENCY(HZ)	OUTPUT VOLTAGE(V)	GAIN	GAIN IN dB

BPF:

INPUT FREQUENCY(HZ)	OUTPUT VOLTAGE(V)	GAIN	GAIN IN dB

BRF:

INPUT FREQUENCY(HZ)	OUTPUT VOLTAGE(V)	GAIN	GAIN IN dB

RESULT:

Thus the various active filter circuits, low pass, high pass, band pass was designed and the frequency response was analysed.

Experiment No: 6

STATIC CHARACTERISTICS OF MOSFET

AIM:

To plot the Transfer and Drain characteristics of MOSFET and determine Trans conductance and output Resistance.

Apparatus:

S.no	Apparatus	Range	Quantity (No)
1	MOSFET	IRF 740	1
2	Resistor	560 Ω	1
3	Ammeter (DC)	0-60mA	1
4	Voltmeter (DC)	0-60V	1
5	Voltmeter (DC)	0-30V	1
6	Multimeter	-	1
7	VRPS	0-30V	3
8	Connecting wires	-	Few

THEORY:

A MOSFET (Metal oxide semiconductor field effect transistor) has three terminals called Drain, Source and Gate. MOSFET is a voltage controlled device. It has very high input impedance and works at high switching frequency.

MOSFET's are of two types 1) Enhancement type 2) Depletion type.

Tabular column:

A) Transfer Characteristics:

V_{DS1} = _____ Volts		V_{DS2} = _____ Volts	
V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)

B) Drain Characteristics:

V_{GS1} = _____ Volts		V_{GS2} = _____ Volts	
V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)

Calculation:

Trans conductance:

$$g_m = \left|\frac{\Delta I_D}{\Delta V_{GS}}\right| = \_\_\_\_\_ mho\ at\ constant\ V_{DS}$$

Out Resistance:

$$R_0 = \left|\frac{\Delta V_{DS}}{\Delta I_D}\right| = \_\_\_\_\_ \Omega\ at\ constant\ V_{GS}$$

PROCEDURE:

A) Transfer Characteristics:

1. Make the connections as per the circuit diagram.
2. Initially keep V1 and V2 at 0 V.
3. Switch ON the regulated power supplies. By varying V1, set VDS to some constant voltage say 5V.
4. Vary V2 in steps of 0.5V, and at each step note down the corresponding values of VGS and ID. (Note: note down the value of VGS at which ID starts increasing as the threshold voltage).
5. Reduce V1 and V2 to zero.
6. By varying V1, set VDS to some other value say 10V.
7. Repeat step 4.
8. Plot a graph of VGS versus ID for different values of VDS.

B) Drain or Output Characteristics:

1. Make the connections as per the circuit diagram.
2. Initially keep V1 and V2 at zero volts.
3. By varying V2, set VGS to some constant voltage (must be more than Threshold voltage).
4. By gradually increasing V1, note down the corresponding value of VDS and ID. (Note: Till the MOSFET jumps to conducting state, the voltmeter which is connected across device as VDS reads approximately zero voltage. Further increase in voltage by V1 source cannot be read by VDS, so connect multimeter to measure the voltage and tabulate the readings in the tabular column).
5. Set VGS to some other value (more than threshold voltage) and repeat step 4.
6. Plot a graph of VDS versus ID for different values of VGS.

Note: If VDS is lower than VP (pinch-off voltage) the device works in the constant resistance region that is linear region. If VDS is more than VP, a constant ID flows from the device and this operating region is called constant current region.

Result:

Transfer and Drain characteristics of MOSFET and determine Trans conductance and output Resistance are studied.

Experiment No.7

FET CHARACTERACTICS

Aim :-

To study the static output and transfer characteristics of a FET (Field Effect Transistor) and to determine the drain resistance, Trans conductance, and amplification factor.

Apparatus:-

Field effect transistor (BFW10), 0-30V (with voltage and current indication),100mA variable DC voltage power supply, potentiometers (0- 1Mohms,0-10 k ohms, and D.C milliammeters (0-50 mA, 0-1mA), Volt meters (0- 50 Volts, 0-5V).

Theory:

FET is a three terminal device. FET's can be characterized in two main categories like JFET(Junction Field Effect Transistor) and MOSFET(Metal Oxide Field semiconductor). Here we study the JFET characteristics. JFET's are further of two types n-channel type and p-channel type.

Main feature of JFET:-

1. It is a uni-polar three terminal device, which solely depends on the conduction of either of electrons or holes.
2. In the operation of this the electric field established by the charges controls the conduction; hence the name Field Effect Transistor.
3. Field Effect Transistor is a voltage control device whereas BJT is a current control device. The output current in the BJT is controlled by the input current level where as the output current in FET is controlled by the applied voltage in the input circuit.
4. There are two types of BJT i.e p-n-p and n-p-n. Similarly FET is of two types p-channel FET and n-channel FET.
5. Gate-source junction is generally reverse biased and gate drain junction is forward biased.
6. The effective channel width, which allows current flow, is controlled by reverse biasing the gate source junction, which changes the width of the space charge in the channel.
7. The reverse bias voltage given to gate- source junction, which just prevents the current flow from the source to drain is called "pinch off voltage".
8. By increasing the drain voltage, drain current increases. At some value of V_D breakdown occurs. Then an avalanche current will flow which is very large. This is called breakdown region.

Parameters of FET:-

1. Dynamic Drain resistance (r_d):-

Dynamic drain resistance at an operating point is defined as the ratio of small change in drain voltage to the corresponding change in the drain current , when the gate voltage is kept constant.

$r_d = (\Delta V_{DS}) / (\Delta I_D)$ V_{GS} being constant.

The typical value of r_d is 200Ω(ohms).

2. Mutual Conductance or Trans conductance (g_m):- The trans- conductance at an operating point is defined as the ratio of a small change in drain current to the corresponding change in gate voltage when drain voltage is kept constant.

$g_m = (\Delta I_D) / (\Delta V_{GS})$ when V_{DS} is constant.

Typical value of g_m is 12mho

3. Amplification Factor (μ):- Amplification factor is defined as the ratio of small change in drain voltage to the corresponding change in gate voltage when drain current is kept constant.

$\mu = (\Delta V_{DS}) / (\Delta V_{GS})$ when I is constant.

μ being the ratio of two voltages it has no units. Typical value of amplification factor of FET is around 1. The above parameters are related by

$\mu = (r_d) \times g_m$

Construction:-

n-channel type JFET starts with n type silicon bar. The two ends of it with attached ohmic constants behave like two terminals called source and drain. Heavily doped p type regions are diffused in to it on either side called gates (see Fig 1). Generally the two gates are connected together.

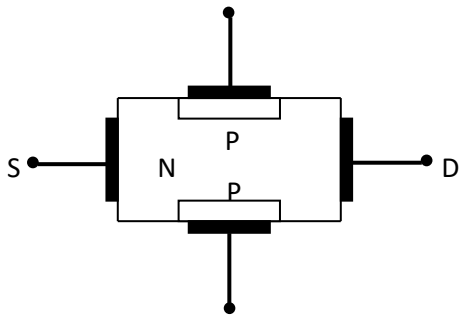


Fig:1

An alternative method of preparation is also there (see FIG 2). A lightly doped n type semiconductor is doped into the p type material, which serves as the channel, and further a heavily doped p type material is doped in to the n type material as shown (see Fig 2).

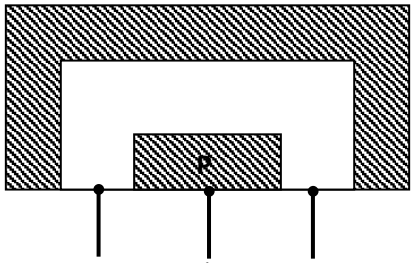


Fig: 2

The drain and the source terminals are taken from n-channel and gate terminal is taken from p type material.

Schematic representation:-

Fig 3shows the schematic representation of FET

Fig: 3

The arrow mark on the gate terminal indicates the direction in which gate current flows when gate junction is forward biased. For n-channel FET arrow is shown is shown into the gate.
For p- channel FET away from gate.

Source:- It is the terminal through majority charge carriers enter the bar.

Drain:- It is the terminal through which majority charge carriers leave the bar.

Gate:- It is the terminal which analogous to base terminal in BJT(Bipolar Junction Transistor) and controls the flow of charge carriers.

Channel:- The region between the source and drain through which majority charge carriers move. The width of this is adjustable by controlling the space charge region in it.

Procedure:-

The connections are made as shown in the circuit diagram (see Fig 4)

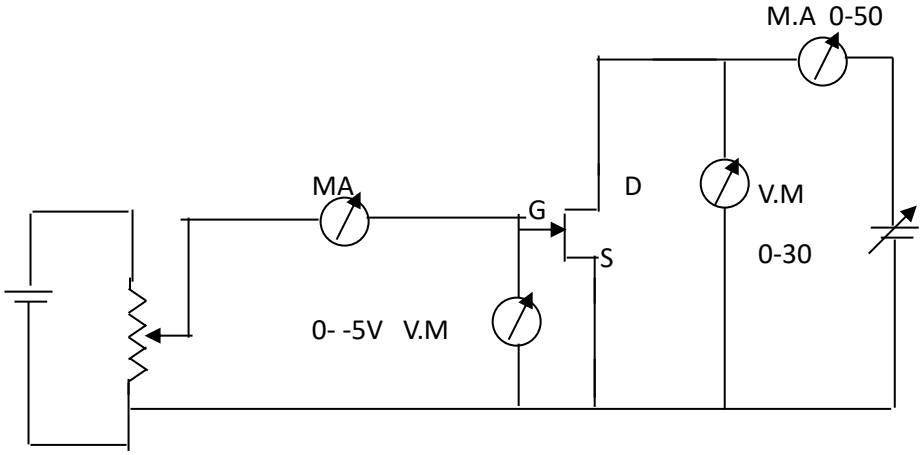


Fig: 4

To draw the o/p characteristics :

V_{GS} is kept initially at zero voltage. V_{DS} is varied and the corresponding values of the I_D are noted. Next V_{GS} is kept at -1V, -2V, …… and then for each value of $V_{GS,}$ the values of I_D corresponding to different value of V_{DS} are noted. These observations are recorded in the tabular form. A graph is plotted between V_{DS} and I_D showing the variation of I_D with

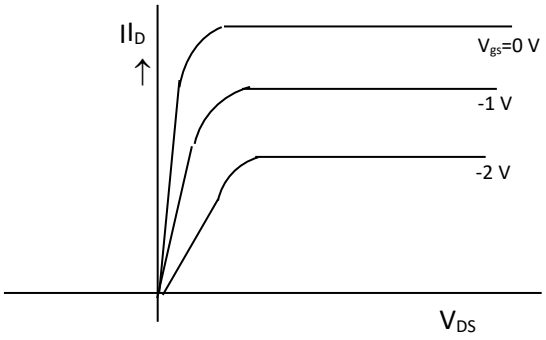


Fig: 5(a)

V_{DS}. Different curves are obtained corresponding to different values of V_{DS} . Those are called output characteristics (see Fig 5a).

To draw the transfer characteristics:-

Keeping the value of V_{DS} constant, varying the (negative) gate voltage in steps the corresponding values of the output current I_D are noted. This procedure is repeated for different values of V_{DS}. Graph is plotted taking V_{GS} on the –ve X-axis and I_D on Y-axis (see FIG 5b).

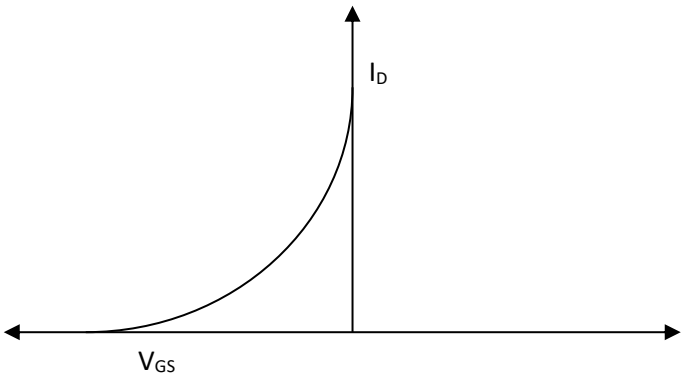


Fig: 5(b)

Observations are recorded in the following tabular forms:

Output characteristics: -

$V_{GS=0V}$		$V_{GS=-1V}$		$V_{GS=-2V}$	
V_{DS} (volts)	I_D(mA)	V_{DS} (volts)	I_D (mA)	V_{DS} (volts)	I_D (mA)

From the output characteristics r_d and μ are determined by taking the ratios $(V_2-V_1)/(I_{d2}-I_{d1})$ And $(V_{d2}-V_{d1})/(V_{g2}-V_{g1})$

Transfer characteristics:-

$V_{DS=4V}$

V_{GS} (volts)	I_D (mA)

Transconductance is determined from the graph from the ratio $(I_{d2}-I_{d1})/(V_{g2}-V_{g1})$

Amplification factor of the FET is determined from the relation $\mu = r_d\, g_m$

Typical values for BFW 10 are r_d= 200Ω; g_m =12 mho; μ = 1

Precautions

1. Before making connections the terminals of the FET are to be correctly identified.
2. Dry soldering is to be avoided.
3. Gate terminal should not be forward biased.
4. The maximum voltage at the gate should not be more than five volts
5. The maximum drain to source voltage for each gate voltage should not exceed
   i. breakdown voltage.
6. Leads of FET should not be touched with hands without proper grounding
7. Current meters must be connected at a point (in series) and voltmeters across any two points of interest following polarity.

Result:

The output and transfer characteristics of a FET are studied and the drain resistance, trans conductance and amplification factor are determined to be

Trans conductance =

Amplification factor =

Drain resistance =